Jianwei Jia

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EDUCATION

Georgia Institute of Technology, US | ECE (Ph.D.) **08/2023 - present**
GPA: 4.0/4.0 Supervisor: Prof. Shimeng Yu
Research Direction: analog and digital circuit design based on Ferroelectric devices

The University of Michigan -Ann Arbor, US |VLSI (M.S.E.) **09/2021 - 04/2023**
GPA: 3.95/4.0 Course: 427, 413, 470, 522, 627

Nankai University, CN |Microelectronics (B.S.) **09/2017 - 06/2021**
GPA: 3.73/4.0 (88.77/100)

RESEARCH & ACADEMIC EXPERIENCE

• Have participated in multiple mixed-signal IC Design and Digital IC design projects

1. Mixed-signal Circuit, Tape-out, and Test

From 08/2023 to 08/2025 Multiple FeFET Tape-outs, Gatech ***Research Assistant***

- Led 3 successful tape-out chips, publications in preparation.

From 01/2024 to 07/2025 Reconfigurable Ferroelectric Bandpass Filter for IEGM ***Research Assistant***

- Designed an ultra-low power reconfigurable bandpass filter based on ferroelectric devices, first established the low-frequency noise model for FeFET devices based on measurement results, and performed circuit-level noise influence analysis.

From 02/2024 to 05/2024 10-bit SAR ADC Tape-out, Gatech

- Designed a 10-bit SAR ADC, including the bootstrapped circuit, 2-stage amplifier, strong-arm comparator, and a digital control block. (PDK: Ti lbc7 PDK, Sponsor: Ti)

From 01/2022 to 08/2022 Secure and Programmable PMU Tape-out, Umich ***Research Assistant***

- Designed a Power Management Unit based on the switched-capacitor DC-DC converter generator under the open-source flow from OpenFASOC and OpenRoad. (PDK: skywater130, Sponsor: Google)

2. Digital Circuit Design

From 10/2022 to 12/2022 N-Way Super-Scalar with Early Branch Resolution, Umich

- Designed an N-way super-scalar with early branch resolution under R10K architecture and RISC-V ISA. Realize the basic function of a CPU, including branch predictors and L1 data cache, and finish structural simulation. Be responsible for the whole architecture-level implementation and reservation station, branch recovery, LSQ, and cache RTL design.

From 10/2021 to 12/2021 Customized Floating-Point Unit, Umich

- Designed a 16-bit floating-point unit to realize addition, subtraction, and multiplication. Implemented booth decoding and Wallace-tree adder structure with a sparse Kogge-Stone Adder to reduce the adding stage and delay of the multiplication instruction. Be responsible for part module design and layout. (PDK: IBM130)

HONORS & AWARDS

Nankai University Innovation Scholarship 11/2020

Nankai University Academic Merit Scholarship 11/2020

The 2nd Prize in the 2019 National Undergraduate Electronics Design Contest 09/2019

PERSONAL SKILLS

Circuit Design Tools: Virtuoso, VCS, Design Compiler, Genus, Innovus, Prime Time, Altium Designer, etc.

Code Class Tools: System Verilog, Tcl, Matlab, Makefile, Python, C++, Linux, Perl, etc.

PUBLICATIONS

Journal

1. **J. Jia**, Z. Jia, O. Phadke, Y. Shi, S. Yu, "**Reconfigurable Ferroelectric Bandpass Filter With Low-Frequency Noise Analysis for Intracardiac Electrogram Monitoring**," in IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (***JXCDC***), vol. 11, pp. 67-73, 2025.
2. M. Vadlamani, **J. Jia**, T. Xie, Y.C. Luo, J. Lee, S. Li, S. Yu, "**Capacitive Crossbar Array for Solving Matrix Equations in One-Shot**," in IEEE Electron Device Letters (***EDL***), vol. 46, no. 3, pp. 389-392, March 2025.

Conference

1. Y. Kong, **J. Jia**, A. Lu, F. Waqar, Y.C. Luo, H. Li, I. Young, S. Yu, "**Digital Compute-in-Memory Ising Annealer with Ferroelectric Capacitor-Based nvSRAM for Combinatorial Optimization Problems**," in 2025 IEEE International Symposium on Circuits and Systems (***ISCAS***), London, UK, 2025.
2. W. H. Huang*, **J. Jia***, Y. Kong, F. Waqar, T. H. Wen, M. F. Chang, S. Yu, "**Hardware Acceleration of Kolmogorov-Arnold Network (KAN) for Lightweight Edge Inference**," in Proceedings of the 30th Asia and South Pacific Design Automation Conference (***ASPDAC***), New York, NY, USA, 2025.
3. **J. Jia**, Z. Jia, O. Phadke, G. Choe, Y. Shi, S. Yu, "**A Reconfigurable Bandpass Filter with Ferroelectric Devices for Intracardiac Electrograms Monitoring**," in 2024 IEEE 67th International Midwest Symposium on Circuits and Systems (***MWSCAS***), Springfield, MA, USA, 2024.